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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER
BRAGDON, REGINALD GLENWOOD

ART UNIT	PAPER NUMBER
2188	7

DATE MAILED: 09/10/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/629,085	DAMRON, PETER C.
	Examiner	Art Unit
	Reginald G. Bragdon	2188

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 August 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Objections

1. Claims 9-27 are objected to because of the following informalities:

As per claim 9, line 9, --a-- should be added before "corresponding".

As per claim 9, line 12, --a-- should be added before "corresponding".

As per claim 12, line 8, --a-- should be added before "corresponding".

As per claim 12, line 17, --a-- should be added before "corresponding".

As per claim 13, line 6, "TLB" should be --TLBs--.

As per claim 13, line 7, "access" should be "address".

As per claim 20, line 16, --a-- should be added before "plurality".

As per claim 21, line 4, --a-- should be added before "corresponding".

All dependent claims are objected to as having the same deficiencies as the claims they depend from.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1, 3, and 6-8 are rejected under 35 U.S.C. 102(b) as being anticipated by Moore et al. (5,437,017).

As per claims 1 and 8, Moore et al. teaches a multiprocessor system, where each processor 10 includes a TLB 40 and each processor is connected to a bus 8 ("main communications network"). See figure 1. The TLB 40 is used to translate a virtual address to an associated real ("physical") address ("accessing a virtual address..." and "locating an associated physical address..."). See column 2, lines 7-11. In response to invalidating an entry in a particular TLB ("said second entry was removed"), a TLB invalidate (TLBI) instruction ("TLB message") is sent to the bus ("sending a TLB message from one of said plurality of processors to said main communication network"; see column 3, lines 5-8) and then to the other processors on the bus ("sending said TLB message from said main communication network to said plurality of processors"). See column 3, lines 8-16.

As per claims 3 and 6-7, Moore et al. teaches that the invalidate instruction is performed as a result of a modification of a translation relationship (i.e. "write access of said second entry" or "comparing said second entry...if said second entry affects said address data stored therein") and therefore all copies of the entry should be invalidated. See column 7, lines 7-18.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1 and 9-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chan et al. (5,524,216) in view of Moore et al.

As per claims 1, 9, 12, and 19-21, Chan et al. teaches a plurality of processors 21-22, 26-27 (figure 1), where each processor includes a cache and a TLB (see column 2, lines 62-66). With reference to figure 1, the system includes a plurality of local buses 20, 25 ("independent paths") connected to central bus 10 ("main communication network"). The TLB in a processor is inherently used in performing a data access. Chan et al. further teaches transmitting transactions between processors over the local buses and the central bus.

Chan et al. does not specifically teach a generating a TLB "message" which is transmitted to other TLBs within the system. Moore et al. teaches that it was known to generate a TLB invalidate instruction ("TLB message") which is broadcast to other processors in a system over a main bus in order to invalidate an entry in a TLB. See column 3, lines 5-11. It would have been obvious to one of ordinary skill in the art to have modified Chan et al. to transmit TLB invalidate coherency instructions between the processors, as suggested by Moore et al., because the transmission of a TLB invalidate instruction would maintain coherency without requiring inter-processor interrupts (see column 2, lines 43-47), thereby improving system performance.

As per claims 10, 14, 17, 22, and 24-25, the combination of Chan et al. and Moore et al. does not teach reading correct data from the page tables in memory on a TLB miss. However, it would have been obvious to one of ordinary skill in the art to have read the correct translation data from main memory on a TLB miss using a read access message from the TLB in order to have maintained efficiency in the system by keeping frequently accessed translations in the TLB.

As per claims 11, 13, 15, 18, 23, and 26-27, Moore et al. teaches that the invalidate instruction is performed as a result of a modification of a translation relationship (i.e. "write access of said second entry" or "comparing said second entry...if said second entry affects said address data stored therein") and therefore all copies of the entry should be invalidated. See column 7, lines 7-18.

As per claim 16, Moore et al. teaches performing a TLB invalidate operation in response to relocating ("moving") data or instructions within system memory. See column 7, lines 13-15.

6. Claims 2 and 4-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Moore et al.

As per claims 2 and 4-5, Moore et al. does not teach reading correct data from the page tables in memory on a TLB miss. However, it would have been obvious to one of ordinary skill in the art to have read the correct translation data from main memory on a TLB miss using a read access message from the TLB in order to have maintained efficiency in the system by keeping frequently accessed translations in the TLB.

Response to Arguments

7. Applicant's arguments filed 18 August 2003 have been fully considered but they are not persuasive.

Applicant argues in the paragraph spanning pages 18-19 of the response filed 18 August 2003 that the TLBI instruction of Moore et al. is not a TLB message generated in response to an operation performed on an associated TLB. However, the TLBI instruction is issued as a result of a relocation of data or instructions within the system memory, or as a result of any other

operation which modifies the translation relationship between the virtual address and the real ("physical") address in system memory. See column 7, lines 13-18. At the very least, the relocation of data or instructions within the system memory ("another location within the computer system") corresponds to (b) set forth by Applicant at lines 13-15 of claim 1. Therefore, Moore et al. teaches that the TLBI instruction is generated in response to an operation performed on the TLB, as set forth in claim 1.

Applicant also argues, on page 19, lines 5-7, of the response that the TLB message includes a code indicating that it is a TLB message, a read/write bit, and the physical address. However, these features are not claimed and therefore it is not relevant that Moore et al. does not teach them.

With respect to the rejection of the claims under 35 U.S.C. 103, Applicant argues that Chan et al. does not teach or suggest the interconnect network having a plurality of independent paths, the plurality of processors being interconnected to each other via corresponding ones of the plurality of independent paths. Applicant appears to be trying to set forth that each processor is connected to another processor via a dedicated one-to-one connection. However, the claim language of "an interconnect network having a plurality of independent paths" does not set forth a plurality of dedicated one-to-one connections between the processors. The structure shown in figure 1 of Chan et al. also teaches a plurality of independent paths, with the processors distributed among the plurality of independent paths and interconnected to each other via a corresponding independent path.

Furthermore, if Applicant intends to set forth in the claim language dedicated one-to-one connections between the processors, Applicant should point out how this language is supported

in the specification. From figure 1 of the present specification, it appears that the processors 14a-14b are not connected via a dedicated one-to-one connection, but are instead connected to a communication network in a manner similar to that shown by Chan et al. in figure 1.

Applicant also argues on page 21 of the response that since an interconnect network is claimed, no bus arbitration or retry is necessary. However, this "feature" is not reflected in the claim language. Applicant further argues that the present invention is more efficient since it does not require executing an instruction, however this is not persuasive since the claim language does not preclude any instruction execution.

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

9. Any response to this final action should be mailed to:

Box AF
Commissioner of Patents and Trademarks
Washington, D.C. 20231

The fax phone numbers for the organization where this application or proceeding is assigned are as follows:

(703) 746-7238 (After Final Communications)

or

(703) 746-7239 (Official Communications)

(703) 746-7240 (For Status inquiries, draft communications)

and/or

(703) 746-5693 (Use this FAX#, only after approval by the Examiner, for "INFORMAL" or "DRAFT" communications. An Examiner may request that a formal page/amendment be faxed directly to them on occasion).

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA., Fourth Floor (receptionist).

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Reginald G. Bragdon whose telephone number is (703) 305-3823. The examiner can normally be reached on Monday-Thursday from 7:00 AM to 4:30 PM and every other Friday from 7:00 AM to 3:30 PM.

The examiner's supervisor, Mano Padmanabhan, can be reached at (703) 306-2903.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-3900.

Reginald G. Bragdon
Primary Patent Examiner
Art Unit 2188

RGB
September 8, 2003